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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/783,626	02/14/2001	Mark Kaplun	100.004US01	2709

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EXAMINER

TRAN, QUOC DUC

ART UNIT	PAPER NUMBER
2643	23

DATE MAILED: 06/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/783,626

Applicant(s)

KAPLUN ET AL.

Examiner

Quoc D Tran

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 27 February 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-34 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 19-34 is/are allowed.
- 6) ☒ Claim(s) 1-17 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>17&18</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Arguments

1. In view of the Appeal Brief filed on 2/27/2004, PROSECUTION IS HEREBY REOPENED. New ground of rejections is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) request reinstatement of the appeal.

If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 7 and 14 are rejected under 35 U.S.C. 102(e) as being anticipated by Ridolfo (6,492,901).

Consider claim 1, Ridolfo teaches an alarm mechanism, comprising: a hardware component, including first and second registers (corresponding to current alarm file 42 and alarm

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status overview module 44; col. 8 lines 40-65), the first register (44) adapted to store a value that indicates a change in state of at least one alarm (col. 8 lines 49-51) and the second register (42) adapted to store current states of each of the at least one alarm (col. 8 lines 53-56, that is, the alarm condition “now”); and a software component, responsive to interrupt requests from the hardware component, adapted to read the first and second registers (col. 8 lines 60-65; col. 9 lines 37-44).

Consider claim 7, Ridolfo teaches an alarm mechanism, comprising: at least one alarm (col. 5 lines 15-18); a first register, responsive to the at least one alarm, and adapted to store a value that indicates a change in state of at least one alarm (corresponding to alarm status overview module 44; see col. 8 lines 40-65); and a second register, responsive to the at least one alarm, and adapted to store current states of each of the at least one alarm corresponding to current alarm file 42; col. 8 lines 40-65).

Consider claim 14, Ridolfo teaches a method for monitoring alarm conditions, the method comprising: receiving an indication of a change in state of an alarm; recording the change in state of the alarm in a first register (col. 8 lines 49-51); recording the current state of the changed alarm in a second register (col. 8 lines 53-56, that is, the alarm condition “now”); and generating an interrupt (col. 9 lines 37-44).

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

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5. Claims 1, 2, 4, 7, 9, 11 and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Le Nay et al (Re: 32,468).

Consider claim 1, Le Nay et al teach an alarm mechanism, comprising: a hardware component, including first and second registers (corresponding to register 164 and register 166; col. 9 lines 30-48) the first register (i.e., register 166) adapted to store a value that indicates a change in state of at least one alarm (col. 9 lines 39-48) and the second register (i.e., current status register 164) adapted to store current states of each of the at least one alarm (col. 9 lines 35-38); and a software component, responsive to interrupt requests from the hardware component, adapted to read the first and second registers (col. 9 lines 44-48 and col. 10 lines 2-7).

Consider claim 2, Le Nay et al did not clearly suggest wherein the first and second registers comprising first and second *n-bit registers* for monitoring n alarms. However, it is inherent since registers or memory or buffers use binary code for storing information.

Consider claim 4, Le Nay et al teach wherein the second register is adapted to store a first value for a first state and second value for a second state (col. 10 lines 56). It should be noted that the status of the alarm is either “on” state or “off” state.

Consider claim 7, Le Nay et al teach an alarm mechanism, comprising: at least one alarm (col. 9 lines 30-31); a first register (i.e., register 166), responsive to the at least one alarm, and adapted to store a value that indicates a change in state of at least one alarm (col. 9 lines 39-48); and a second register (i.e., register 164), responsive to the at least one alarm, and adapted to store current states of each of the at least one alarm (col. 9 lines 35-38).

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Consider claim 9, Le Nay et al did not clearly suggest wherein the first and second registers comprise first and second **n-bit registers** for monitoring n alarms. However, it is inherent since registers or memory or buffers use binary code for storing information.

Consider claim 11, Le Nay et al teach wherein the second register is adapted to store a first value for a first state and a second value for a second state (col. 10 lines 56). It should be noted that the status of the alarm is either “on” state or “off” state.

Consider claim 14, Le Nay et al teach a method for monitoring alarm conditions, the method comprising: receiving an indication of a change in state of an alarm; recording the change in state of the alarm in a first register (col. 9 lines 39-48); recording the current state of the changed alarm in a second register (col. 9 lines 35-38); and generating an interrupt (col. 9 lines 44-48 and col. 10 lines 2-7).

6. Claims 5-6, 8, 12-13, 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Le Nay et al (Re: 32,468) in view of Renaudin et al (4,388,715).

Consider claims 5 and 12, Le Nay et al did not clearly suggest wherein the second register is adapted to store a first **logic value for an alarm state** and a second **logic value for a non-alarm state**. However, Renaudin et al suggest an alarm logic having logic “1” and “0” for alarm and non-alarm condition (col. 3 lines 1-3). Therefore, it would have been obvious to one of the ordinary skill in the art at the time the invention was made to utilize the teaching of Renaudin et al into view of Le Nay et al in order signify whether the alarm status has change or not.

Consider claims 6, 13 and 16, Le Nay et al did not clearly suggest wherein the first register is adapted to store a first value in **a bit location** of the first register upon one or more changes in state of the corresponding alarm indicator. However, Renaudin et al teach alarm logic

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for signifying an alarm condition by transmission of a bit (col. 3 lines 1-3). Therefore, it would have been obvious to one of the ordinary skill in the art to incorporate the teaching of Renaudin et al into view of Le Nay et al to signify the alarm condition.

Consider claims 8 and 15, Renaudin et al teach the alarm logic for used in a digital switch exchange for detecting plurality of alarms. Renaudin and Le Nay et al did not further suggest wherein the alarm logic for a serial line on the backplane of an access device and to receiving an indication of an alarm condition in a serial line on a backplane of an access device. However, it would have been obvious to one skill in the art to recognize that the digital switch exchange would obviously include a serial access port for access to determine fault conditions. Therefore, it would have been obvious to one of the ordinary skill in the art at the time the invention was made to incorporate such teaching in order to detect alarm therein.

Consider claim 17, Le Nay et al did not clearly suggest wherein recording the current state comprises recording a first logic value in a *bit location* of the second register. However, Renaudin et al teach alarm logic for signifying an alarm condition by transmission of a bit (col. 3 lines 1-3). Therefore, it would have been obvious to one of the ordinary skill in the art to incorporate the teaching of Renaudin et al into view of Le Nay et al to signify the alarm condition.

Claim Rejections - 35 USC § 102

7. Claims 1, 2, 4-7, 9-14 and 16-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Kusyk et al (5,920,258).

Consider claim 1, Kusyk et al teach an alarm mechanism, comprising: a hardware component (Fig. 1), including first and second registers (Fig. 1; corresponding to alarm register

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22 and event register 26) the first register (i.e., event register 26) adapted to store a value that indicates a change in state of at least one alarm (col. 3 lines 16-20) and the second register (i.e., alarm register 22) adapted to store current states of each of the at least one alarm (col. 3 lines 6-11); and a software component, responsive to interrupt requests from the hardware component, adapted to read the first and second registers (col. 3 lines 40-45).

Consider claim 2, Kussyk et al did not clearly suggest wherein the first and second registers comprising first and second *n-bit registers* for monitoring *n* alarms. However, it is inherent since registers or memory use binary code for storing information.

Consider claim 4, Kussyk et al teach wherein the second register is adapted to store a first value for a first state and second value for a second state (col. 3 lines 17-20).

Consider claim 5, Kussyk et al teach wherein the second register is adapted to store a first logic value for an alarm state (i.e., active or hi) and a second logic value for a non-alarm state (i.e., inactive or lo) (col. 3 lines 8-10).

Consider claim 6, Kussyk et al teach wherein the first register is adapted to store a first value in a bit location of the first register upon one or more changes in state of the corresponding alarm indicator (col. 3 lines 16-20).

Consider claim 7, Kussyk et al teach an alarm mechanism, comprising: at least one alarm (col. 2 lines 65-67); a first register (i.e., event register 26), responsive to the at least one alarm, and adapted to store a value that indicates a change in state of at least one alarm (col. 3 lines 16-20); and a second register (i.e., alarm register 22), responsive to the at least one alarm, and adapted to store current states of each of the at least one alarm (col. 3 lines 6-11).

Consider claim 9, Kusyk et al did not clearly suggest wherein the first and second registers comprise first and second *n-bit registers* for monitoring *n* alarms. However, it is inherent since registers or memory use binary code for storing information.

Consider claim 11, Kusyk et al teach wherein the second register is adapted to store a first value for a first state and a second value for a second state (col. 3 lines 17-20).

Consider claim 12, Kusyk et al teach wherein the second register is adapted to store a first logic value for an alarm state (i.e., active or hi) and a second logic value for a non-alarm state (i.e., inactive or lo) (col. 3 lines 8-10).

Consider claim 13, Kusyk et al teach wherein the first register is adapted to store a first value in a bit location of the first register upon one or more changes in state of the corresponding alarm indicator (col. 3 lines 16-20).

Consider claim 14, Kusyk et al teach a method for monitoring alarm conditions, the method comprising: receiving an indication of a change in state of an alarm (col. 3 lines 11-17); recording the change in state of the alarm in a first register (col. 3 lines 17-20); recording the current state of the changed alarm in a second register (col. 3 lines 6-11); and generating an interrupt (col. 3 lines 40-45).

Consider claim 16, Kusyk et al teach wherein recording the change in state comprises recording a first logic value in a bit location of the first register (col. 3 lines 16-20).

Consider claim 17, Kusyk et al teach wherein recording the current state comprises recording a first logic value in a bit location of the second register (col. 3 lines 8-11).

8. Claims 3, 10 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kusyk et al (5,920,258).

Consider claims 3 and 10, Kusyk et al did suggest wherein the alarm circuit further including a monitoring to detect alarm conditions and to report alarm condition to the hardware component (col. 2 line 61 – col. 3 line 2). Kusyk et al did not suggest wherein the monitoring circuit adapted to monitor *serial lines on a backplane of an access device*. Because, Kusyk et al patent is issued to Northern Telecom, it would have been obvious to one skill in the art to recognize that the invention is intended for use in a telecommunication system. Although, Kusyk et al did not specifically suggest the monitoring circuit adapted to monitor serial lines on a backplane of an access device. It would have been obvious to one skill in the art to recognize that the monitoring circuit can easily implement to detect fault in the line cards (i.e., serial line) of the telecommunication network. Therefore, it would have been obvious to one of the ordinary skill in the art at the time the invention was made to incorporate such teaching in order to detect alarm therein.

Consider claim 15, Kusyk et al did not further suggest wherein receiving an indication of a change in state of an alarm comprises receiving an indication of an alarm *condition in a serial line on a backplane of an access device*. Because, Kusyk et al patent is issued to Northern Telecom, it would have been obvious to one skill in the art to recognize that the invention is intended for use in a telecommunication system. Although, Kusyk et al did not specifically suggest that the alarm signal received is for the alarm condition in a serial line backplane of an access device. It would have been obvious to one skill in the art to recognize that the alarm circuit can be easily implement to detect fault in the line cards (i.e., serial line) of the telecommunication network. Therefore, it would have been obvious to one of the ordinary skill

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in the art at the time the invention was made to incorporate such teaching in order to detect alarm therein.

Allowable Subject Matter

9. Claim 18 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
10. Claims 19-34 are allowed.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.
12. Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

Facsimile responses should be faxed to:

(703) 872-9306


Hand-delivered responses should be brought to:


Crystal Park II, 2121 Crystal Drive
Arlington, VA., Sixth Floor (Receptionist)

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Quoc Tran** whose telephone number is **(703) 306-5643**. The examiner can normally be reached on Monday-Thursday from 8:00 to 6:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Curtis Kuntz**, can be reached on **(703) 305-4708**.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the **Technology Center 2600** whose telephone number is **(703) 306-0377**.

QUOCTRAN
PRIMARY EXAMINER
AU 2643
May 26, 2004 


CURTIS KUNTZ
SUPERVISOR, PATENT EXAMINER
TECHNOLOGY CENTER 2600